The CSI Chip – A CMOS Charge Successive Integrator with Wide Dynamic Range for the Telescope Array Project

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Abstract

A charge successive integrator (CSI) VLSI with wide dynamic range has been developed for front-end electronics of the Telescope Array project. The CSI has more than 14-bit dynamic range and successively integrate the charge from photo-multiplier tube every 200ns. We have newly designed offset-compensated charge integrator to reduce the offset voltage and the 1/*f* noise. We expect that the offset voltage and the maximum 1/*f* noise can be reduced to less than 1mV and 5mV respectively with this technique. The prototype CSI chip was fabricated in a 0.6μm commercially available CMOS technology. The test results of the prototype CSI chip, which has no offset compensation, are compared to the offset-compensated low-1/*f* noise CSI to confirm the effectiveness of this technique.

I. Introduction

A giant array of air fluorescence detectors using 100 thousands of photo-multiplier tubes (PMT) will be constructed to study highest energy cosmic rays by the Telescope Array project [1]. A CMOS integrated circuit has been developed for the front-end electronics of the DSP-based pipelined data acquisition system in the Telescope Array detector [2]. A charge integration of the signal from PMT is essential in a calorimetric measurement. We integrated four channels of high precision charge integrators with wide dynamic range into a CMOS chip. The chip has been designed and fabricated in the ROHM double-poly triple-metal 0.6μm CMOS process.

The charge integrators must have 12-bit resolution with 16-bit dynamic range, and is also required continuous charge-to-voltage conversion every 200ns to digitize by a pipelined ADC [2]. To satisfy these requirements we have designed a charge successive integrator (CSI) with the two-range input for coarse and fine range. The signal fed into the fine-range input is amplified 16 times by a low-noise bipolar op-amp outside the CSI chip. On the other hand, the coarse-range signal is directly input through an outside unity-gain amplifier.

In the TA data acquisition system, low-frequency baseline fluctuation is monitored by a DSP and is digitally subtracted from the charge-integrated signal. It is, however, too much load to subtract the CSI offset and 1/*f* fluctuation in each sample clock. Hence, we have decided to study a reduction technique of the offset voltage and the 1/*f* noise generated from the CSI itself.

We will present the CSI architecture for this project in the next section, following the offset-compensated and low 1/*f* noise integrator circuit originally designed for this project. We also present the detail of the integrator circuit and the clocking technique. Finally we discuss the result from a SPICE simulation and a chip test.

II. Charge Successive Integrator Architecture

The charge successive integrator (CSI) integrates an input charge within one clock period, and continuously outputs an integrated voltage every clock period.

Figure 1 shows the schematic design of the charge successive integrator, which consists of four active integrators and switches. Each integrator is operated circularly at Sample, Read, Precharge, or Discharge state. A signal at the Read state is output and used for digitization. In this scheme we realize the continuous charge-to-voltage conversion.

Since the integrators have a gain and an offset, the different offset voltage among op-amps causes crucial dispersion of the output voltage. We have resolved this problem to design an offset-compensated charge integrator. Fortunately, this type of integrator also reduces the *1/f* noise of the circuit that is the main noise source of CMOS circuits.

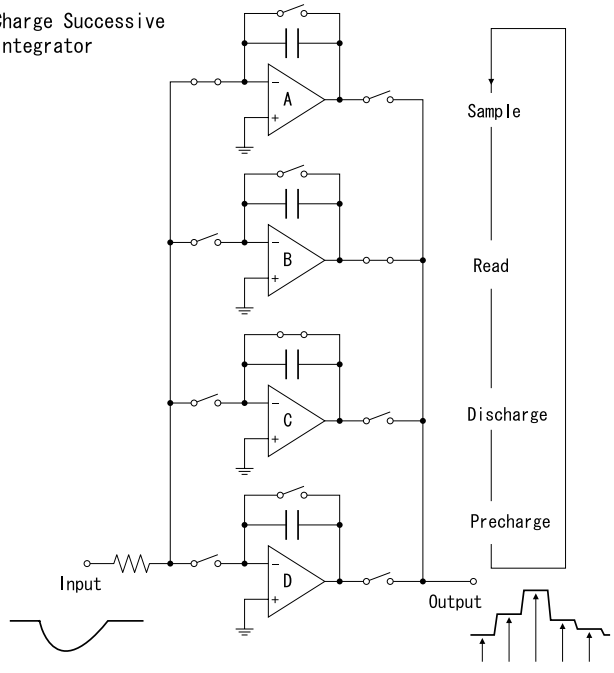

Figure 1: Schematic design of Charge Successive Integrator

Figure 2 shows the schematic diagram for single channel CSI block. The charge signals of x1 and x16 input are fed into coarse and fine CSI block, respectively. A comparator alternates the ranges by comparing between the fine CSI output and threshold voltage V_{th}. If the fine CSI output is greater than the threshold voltage, e.g. the maximum output voltage at fine range, then the CSI output is switched to the coarse CSI output.

Since we expect the noise level outside the chip is much smaller than the inside, the input signal of the fine CSI is amplified outside by using low-noise bipolar circuit. We increase the dynamic range at a gain of 4-bit in this two-range architecture.

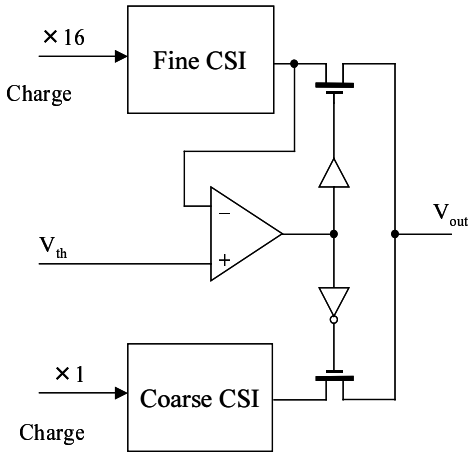

Figure 2: Charge Successive integrator architecture with two-range input.

III. Offset-compensated Charge Integrator

A. Charge Integrator Circuit

Correlated double-sampling techniques are generally used for highly accurate gain amplifier, sample and holds, and integrator [3,4]. It is important to apply this technique for reducing op-amp offset voltage and 1/*f* noise. We designed an applicable circuit to our charge successive integrator with an offset compensation method as a modification of this technique.

Figure 3 shows a schematic of the offset-compensated charge integrator circuit. As finding from the figure, we have used many switches in addition to ordinary charge integrator circuit. An integrating capacitor C and a discharge switch SW_9 are the same as an ordinary charge integrator circuit. In addition to these switches we use the switches SW_2, SW_3, SW_5, SW_6, SW_7, SW_8 setting to be precharge state. The switches SW_1 and SW_4 are used for setting to be sampling and reading state, respectively. We use poly-to-poly capacitance for the integrating capacitor *C*.

The sizes of the switches are listed in table 1. We use three types of CMOS transmission gate, i.e. high-resistance switch for SW_6, normal-resistance switches for SW_4 and SW_9, and low-resistance switches for the others. The reason for using low-resistance switches SW_2 and SW_3 is to reduce the time constant when SW_6 is turned on. We also used the same size switches for SW_5, SW_7, and SW_8 as for SW_2 and SW_3 because of the channel charge cancellation. Since SW_2 and SW_3 turn on when SW_5, SW_7, SW_8 turn off, the channel charge is canceled each other in the neighbor switches. We also use half size of dummy switches for SW_1 and SW_6 not only to cancel the channel charge but also to suppress the effect of clock feedthrough.

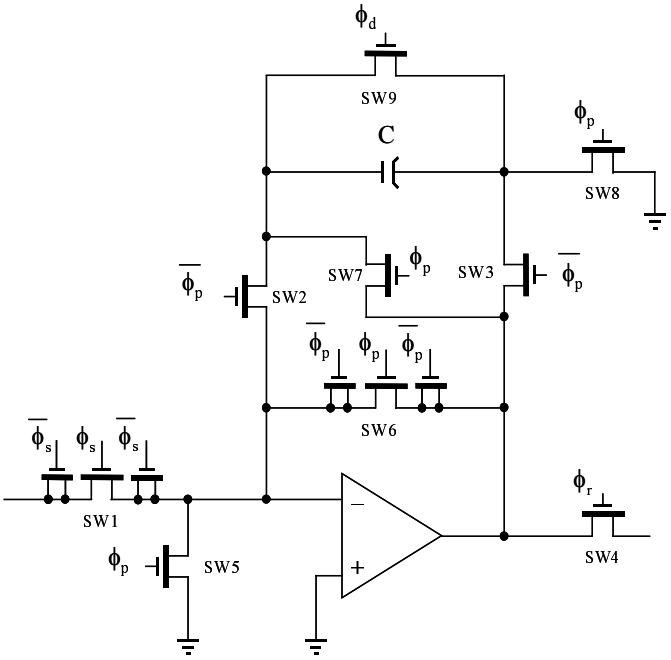

Figure 3: Offset-compensated Charge Integrator circuit.

Table 1: Complementary switch parameter. W and L are the designed gate width and length of unit transistor, respectively. M is the number of multiple-gates.

	NMOS			PMOS			R (ohm)
	W (um)	L (um)	M	W (um)	L (um)	M	
SW1 SW2 SW3 SW5 SW7 SW8	6.75	0.9	6	16.6	0.9	8	100
SW6	3.6	0.9	1	11.4	0.9	1	1200
SW4 SW9	3.6	0.6	1	11.4	0.6	1	850

B. Method of Offset Compensation

The precharge state is added to compensate the op-amp offset. Figure 4 shows the circuit diagram of precharge state, where V_{off} indicates the input-referred offset voltage of the op-amp.

At the precharge state, the switches SW_5, SW_6, SW_7 and SW_8 turn on. An amplified offset voltage V_{op} is determined by the ratio of R_{SW6}/R_{SW5}, and charges the integrating capacitor *C* up to Q_p. The ratio of R_{SW6}/R_{SW5} is set to be about 12 by using the on-resistance of CMOS transmission gate. Since we may change the reference voltage of the op-amp, GND symbol in the figure, according to input voltage range, this ratio should be reasonably constant independent of the input voltage. We

have confirmed the error of the ratio to be less than 1.5% in the SPICE simulation, which is the same level as the fabrication error. The characteristic of the transmission gate is shown in figure 5.

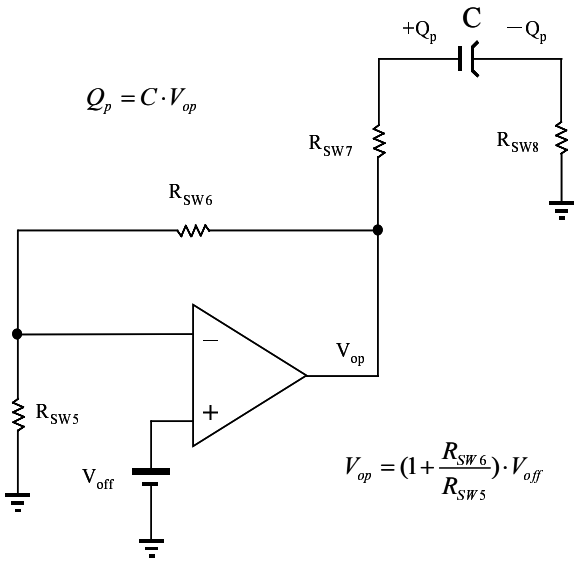

Figure 4: Circuit diagram of precharge state.

Figure 6 shows the circuit diagram at the sample state. The switches SW_2 and SW_3 connect the integrating capacitor in opposite polarity to that at the precharge state. Hence, the sampled charge Q_s becomes

$$Q_s = -\frac{V_{off} - V_i}{R_i + R_{SW1}} \cdot T + Q_p \qquad (1)$$

where T is the sampling interval. If we compensate the offset voltage V_{off}, we need to satisfy

$$Q_p = C \cdot (1 + \frac{R_{SW6}}{R_{SW5}}) \cdot V_{off} = \frac{V_{off}}{R_i + R_{SW1}} \cdot T \qquad (2)$$

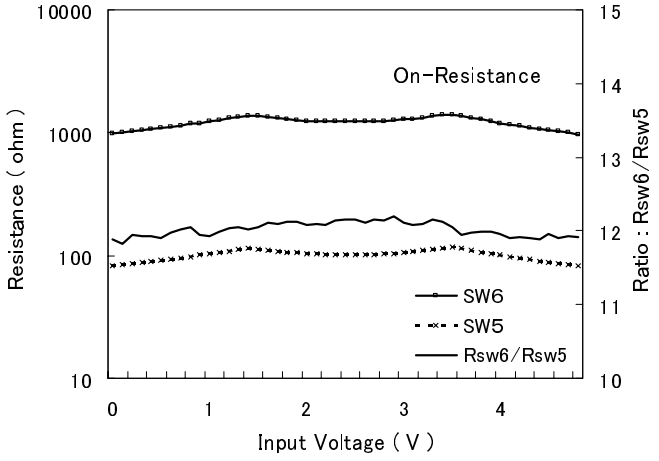

Figure 5: On-resistance of the complementary switches. Ratio of the resistance R_{SW6} to R_{SW5} is set to 12 and to be flat as the function of input voltage.

Since we have chosen C=26pF, R_{SW6}/R_{SW5} =12, T=200ns and R_{SW1}=100Ω, the input resistance R_i is calculated to be 490Ω. Thus we can adjust the cancellation parameters only using input resistance R_i even in case of changing the sampling interval. Since these parameters are also influenced from the parasitic capacitance and resistance, a readjustment of R_i should be made. Note that a change of the input resistance R_i, however, influences the gain of charge integrator as

$$V_{os} = \frac{T}{C \cdot (R_i + R_{SW1})} \cdot V_i \qquad (3)$$

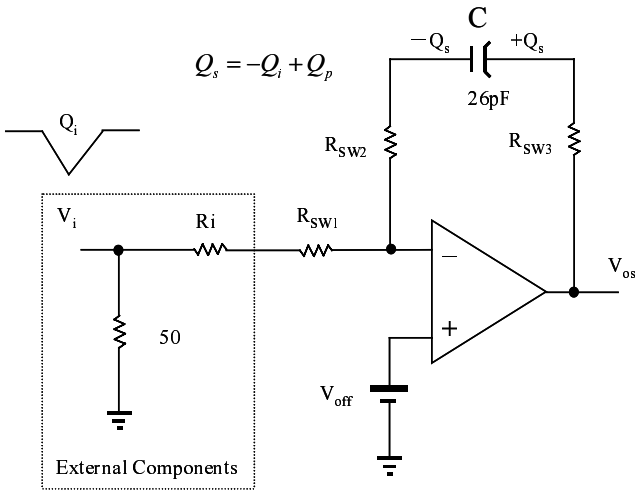

Figure 6: Circuit diagram of sample state.

C. Clock Generator Circuit for the Switches

A 4-bit ring counter generates clocks for the switches. The timing of the clocks is precisely controlled to reduce charge leakage, which severely affects the accuracy of the offset compensation. It is, however, natural that the clock in the actual system has jitter and inaccuracy. For this reason, we have designed a tolerant clock system against the charge leakage as shown in figure 7.

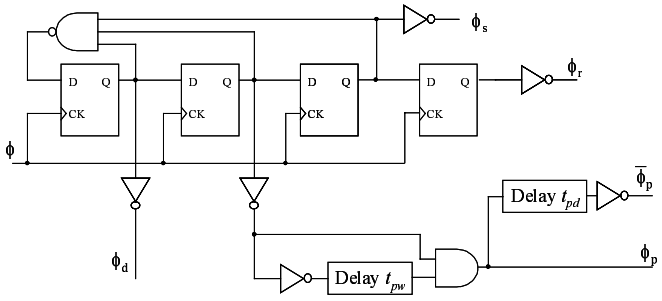

Figure 7: Clock generator for the switches.

Figure 8 shows the timing diagram of the clocks. To reduce leakage current, the precharge clock ϕ_p turns off $T - t_{pw}$

before the sampling clock ϕ_s turns on. A switching delay t_{pd} is needed to avoid the short circuit through SW_2 and SW_3.

Since the sampling time T is 200 ns in our system, we have designed a precharge time t_{pw} = 170±5ns and a switching delay t_{pd} = 7.5±2.5ns. We have confirmed by SPICE simulation that the error of the offset compensation is less than 1mV with these values. The leakage current suddenly increases at t_{pw} > 180ns, while the 1/*f* noise gradually increases at t_{pw} < 160ns. Fortunately, it is easy to control the timing of the switching delay and precharge time within ±2.5ns and ±5ns respectively, using gate delay elements in the CSI chip.

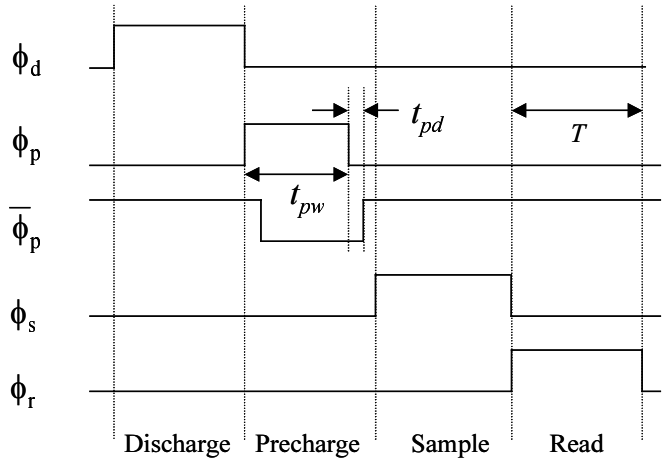

Figure 8: Timing diagram of the switch control.

IV. RESULTS

A. Charge Integration Range

We have designed a wide dynamic range integrator by using the fine and coarse CSI. Figure 9 shows the CSI output voltage as a function of input charge. The fine range, indicated as the steeper dotted line, is switched to coarse range at 4.5V indicated as the solid line. The bottom voltage of the solid line, i.e. switching voltage, is 1.26V. We can reduce the voltage by changing the gain factor, now 16, of outside sub-range amplifier.

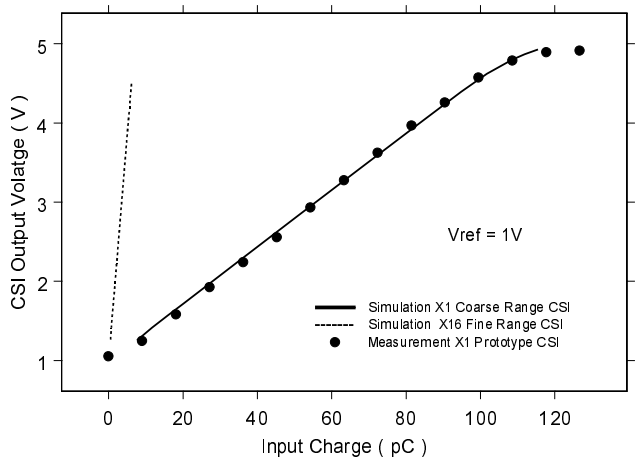

Figure 9: CSI output voltage for fine and coarse range. Black dots are the data from the prototype CSI.

The lines are the result of SPICE simulation, while the black dots are measured data of the coarse range from the prototype CSI fabricated in the same process. Both the data indicate the linearity up to about 4.5V. The CSI chip is operated at 5V power supply and at 1V reference voltage in this measurement. The acceptable input signal range is down to 350mV, i.e. up to 650mV pulse height, without distortion at 1V reference voltage.

B. Offset Voltage

The offset voltage V_{off} of the op-amps charges the integrating capacitor, so that the CSI output voltage is gained by the factor of equation (3) as same as the input voltage V_i.

Figure 10 shows the offset voltage of the CSI output as a function of the op-amp offset voltage. As shown in the figure, CSI offset is gained about 10 without the offset compensation, while its offset is reduced to less than 1mV after the compensation. The black dots are the measured data using 20 samples of the prototype CSI, which has no compensation circuit. Note that the op-amp offset voltages of the prototype CSI are not measured but scaled on the simulation line. Using this plot, we obtain a sample of the offset distribution of the op-amp. Consequently, we estimate the CSI offset voltage is less than 1mV with the compensation circuit even if the op-amp offset is dispersed by process variation.

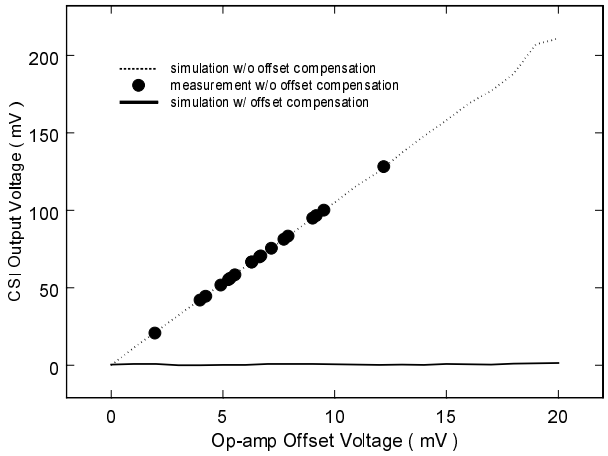

Figure 10: Offset voltage of the CSI output as a function of op-amp offset voltage.

We use the input resistance R_i =520Ω, the precharge time t_{pw} = 170ns and the switching delay t_{pd} = 5ns in the SPICE simulation. If we increase the time to t_{pw} = 180ns and t_{pd} = 10ns, the CSI offset voltage increases to over 10mV. If we set t_{pd} = 0ns, the CSI offset slightly increases. From these results, we set the precharge time t_{pw} = 170±5ns and a switching delay t_{pd} = 7.5±2.5ns.

C. Noise

Root spectral density of the CSI output noise was measured by using FFT analyzer. Figure 11 shows the root-mean-squared voltage of the noise in the prototype CSI, where the broad peak indicates 1/*f* noise from the circuit. Ignore the sharp peak at 1.25MHz because of an aliasing from the 5MHz system clock. The corner frequency of the 1/*f* noise is about 750kHz and the 1/*f* noise reaches to 20mV at 250kHz. The thermal noise is less than 1mV rms.

We simulated the output noise assuming an input-referred noise distribution for both the prototype CSI and the offset-compensated CSI. The 1/*f* noise of the offset-compensated CSI is reduced to less than 5mV all over the frequency.

The 1/*f* noise is gradually reduced if closer t_{pw} to clock period T is used. The 1/*f* noise drops to less than 4mV in the best case of the simulation at t_{pw} = 200ns and t_{pd} = 0ns. On the contrary, if we use such large t_{pw}, the offset voltage increases. From these results, we compromise on the precharge time t_{pw} = 170±5ns and the switching delay t_{pd} = 7.5±2.5ns.

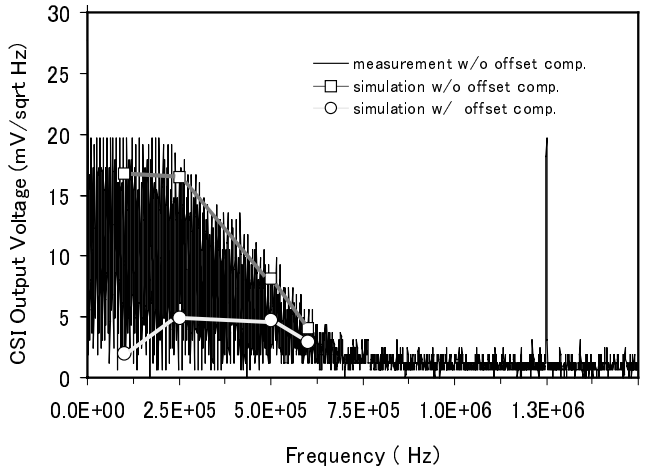

Figure 11: Root spectral density of the CSI output noise.

V. Conclusions

We have developed the charge successive integrator (CSI) with wide dynamic range for the Telescope Array project. To obtain the wide dynamic range, we have developed not only the two-range CSI but also the offset-compensated integrator circuit.

We measured the noise level of the prototype CSI (figure 12) as the reference without offset compensation, and also simulated the noise level of the offset-compensated CSI using SPICE. The maximum noise level is about 20mV in the frequency range below 250kHz without offset compensation, and is 4.8mV in the frequency range from 250kHz to 500kHz with offset compensation.

The offset voltage increases more than 100mV without the offset compensation, while it is less than 1mV with offset compensation. The output range of the CSI is from 1V to 4.5V at 1V reference voltage. Since the two-range CSI magnifies dynamic range by 16 times (4-bit), we expect to achieve around 14-bit dynamic range. If we use a large gain ~700 for the outside sub-range amplifier, we ideally expect 18-bit dynamic range. This calculation completely depends on the noise level of the sub-range amplifier, which is placed outside the CSI VLSI, planning to use bipolar low-noise op-amp.

The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by ROHM Corporation and Toppan Printing Corporation.

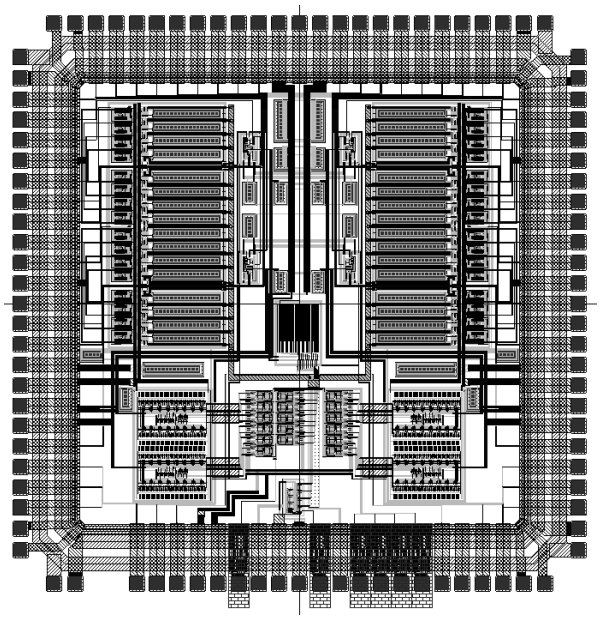

Figure 12 : Layout picture of the prototype CSI implemented on a 3.9 x 3.9mm^2 die using the ROHM double-poly triple-metal 0.6μm CMOS process.

VI. References

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